REMARKS

Claims 1-6 and 11-28 are pending. Reconsideration of the application is respectfully requested based on the following remarks.

I. ALLOWED SUBJECT MATTER

Applicant acknowledges with appreciation the allowance of claims 1-6, 11-18 and 25-27.

II. REJECTION OF CLAIMS 19, 23-24 and 28 UNDER 35 U.S.C. § 103(a)

Claims 19, 23-24 and 28 were rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Publication No. US 2004/00208314 A1 to Patariu et al. (Patariu) in view of US Patent Publication 2005/0160050 A1 to Payne. Withdrawal of the rejection is respectfully requested for at least the following reasons.

i. Neither Patariu nor Payne teach or suggest a network interface device comprising a bus interface coupled with a host bus, and a media access control system coupled with the network and adapted to transfer data between the network interface device and the network as recited in claim 19.

Interface 506 of Fig. 5 of Patariu, as cited, can not adequately represent the bus interface (*e.g.*, 9 of Fig. 1E) of the present invention, as the interface 506 of Patariu is not ***coupled with a host bus in the host system*** (*e.g.*, 7) as recited in independent claim 19. Also, Memory 508 of Fig. 5 of Patariu, as cited, can not constitute the MAC system (*e.g.*, 10 of Fig. 1E) of the present invention, as it does not ***operate to transfer data between the network interface device*** (*e.g.*, 6) ***and the network*** (*e.g.*, 8) as recited in claim 19. Further, if CPU interface 506 of Fig. 5 of Patariu is cited to represent the bus interface (*e.g.*, 9 of Fig. 1E of the present invention), then Memory 508 of Fig. 5 of Patariu is not adapted to ***transfer data between the network interface device*** (comprising the bus interface 506) and the network. The network interface device of the present invention further comprises *a* ***single DES engine*** (*e.g.*, 5a)

operable to perform 3DES processing by selectively feeding back intermediate data results to an input (*e.g.*, 5b) ***thereof...*** Patariu does not discuss or suggest feeding back intermediate data results to an input. Applicant has rigorously reviewed the teachings of Patariu, and have found no such teaching therein. The Office Action makes a general statement that the reference teaches this feature. If this rejection is maintained, applicant respectfully requests further details regarding where in the cited art this feature resides.

The Office Action concedes that Patariu fails to disclose a bus interface and a MAC system as claimed, but asserts that Payne teaches these features. It is respectfully submitted however, that Payne does not teach or suggest a bus interface as cited, which can not adequately represent the bus interface (*e.g.*, 9 of Fig. 1E) of the present invention, as it is not ***coupled with a host bus in the host system*** (*e.g.*, 7) as recited in claim 19, nor does Payne recite a network interface device (*e.g.*, 6 of Fig. 1E of the present invention) ***comprising this bus interface*** as recited in claim 19. Also, modem 28 of Fig. 1 of Payne, as cited, can not constitute the MAC system (*e.g.*, 10 of Fig. 1E) of the present invention, as it is not ***a component within the network interface device*** (*e.g.*, 6) as recited in claim 19, if network interface 20 of Fig. 1 of Payne is used to represent the network interface device (*e.g.*, 6).

In addition, if network interface 20 of Fig. 1 of Payne is cited to represent the network interface device (*e.g.*, 6 of Fig. 1E of the present invention), and the transaction network 16 or the land phone lines 24 of Fig. 1 of Payne is cited to represent the network (*e.g.*, 8 of Fig. 1E of the present invention), then modem 28 of Fig. 1 of Payne is not ***adapted to transfer data between the network interface device*** (as a part of ATM processor 18) **and the network**.

Accordingly, not all features of independent claim 19 are disclosed by Patariu, or Patariu in view of Payne, and withdrawal of the rejection is respectfully requested.

ii. Neither Patariu nor Payne teach or suggest a method of 3DES processing comprising transferring data between the network interface device and the host system using a bus interface, transferring data utilizing a media access control system or performing security processing using a single DES engine as recited in claim 23.

The CPU interface 506 cited for Patariu in Fig. 5 can not represent the **bus interface** (*e.g.*, 9) of the network interface device (*e.g.*, 6 of Fig. 1E) of the present invention as the bus interface 506 which controls the bus can not transfer data to the host system (*e.g.*, 7) from this bus, and Payne discusses no interface bus for ***transferring the outgoing data from the 3DES processing circuit*** (*e.g.*, 5) ***to the network interface device*** (*e.g.*, 6), because the 3DES processing of Payne is done at the host 14 of Fig. 1 (see 3DES item 36). Further, memory elements 508a and 508b of Patariu can not represent the **media access control system** (*e.g.*, 10) as they do not control the transfer of data between a network interface device and a network, and the modem 28 of Fig. 1 of Payne can not represent the **media access control system** (*e.g.*, 10) as it does not control ***transferring the outgoing data from the interface bus*** (*e.g.*, 9) ***to the network*** (*e.g.*, 8 of Fig. 1E of the present invention), because the interface 26 of the host 14 is on the wrong side of the network 16 of Fig. 1 of Payne to transfer ***outgoing data from the interface bus*** (*e.g.*, 9) ***to the network*** (*e.g.*, 8 of Fig. 1E of the present invention). Finally, Patariu does not discuss **using a single DES engine** (*e.g.*, 5a) to perform security processing in a 3DES processing circuit.

Accordingly, not all features of independent claim 23 are disclosed by Patariu, or Patariu in view of Payne, and withdrawal of the rejection is respectfully requested.

III. PREVIOUSLY PRESENTED CLAIM 28

Previously presented claim 28 has several features therein that have been held to be allowable in previously presented claim 1, and is thus believed to be patentable over U.S. Publication No. US 2004/00208314 A1 Patariu et al. (Patariu) or Patariu in view of Payne for at least the following reasons.

Claim 28 comprises *a* ***select switch*** (*e.g.*, 24 of Fig. 1F of the present invention) ***coupled to*** *the data input (e.g., 26* of Fig. 1F*) of the security processing circuit, the data output (e.g., 23), and* ***the data input node*** *(e.g., 25* of Fig. 1F*)* ***of the single DES engine*** (*e.g.*, 5a of Fig. 1E or 21 of Fig. 1F)*, the select switch adapted to selectively couple one of the data input (e.g., 26) and the intermediate result to the data input node of the single DES engine.* As will be shown below, the cited references do not teach all of the above features.

i. Neither Patariu nor Payne teach or suggest a select switch having a connection to the data input node of the single DES engine essential for intermediate result processing as recited in claim 28.

Although Patariu (US Pub. US 2004/00208314 A1) is cited as having a select switch/Mux, item 210 of Fig. 2, this switch explicitly has **no connection** to the **data input node of the single DES engine** (*e.g.*, 5a of Fig. 1E or 21 of Fig. 1F), to provide "feedback" essential for **intermediate result processing** using a single DES engine. Thus, Patariu is also not **adapted to selectively couple one of the data input** *(e.g., 26* of Fig. 1F*)* and the **intermediate result to the data input node** *(e.g., 25* of Fig. 1F*)* of the single DES engine (*e.g., 21* of Fig. 1F). Mux 210 is not connected or adapted to *couple one of the data input and the intermediate result to the data input node of the engine* (DES or 3DES), and the Key & Encryption/Decryption Select (212 of Fig. 2 of Patariu) is not connected or coupled to the **data output** of the single DES engine (single DES or 3DES) as required of the **data select switch** of claim 28 (or the previously presented claim 1). Instead, Key & Encryption/Decryption Select 212 of Patariu is adapted to couple input data to the **keys input** of the 3DES block (208 of Fig. 2).

ii. Neither Patariu nor Payne teach or suggest a feedback path internal to the 3DES block engine essential for intermediate result processing as recited in claim 28.

The "feedback path" cited in Fig. 1 of Patariu between output FIFO block 110 and input FIFO block 108, ***is not a feedback path***, but is instead is described in paragraph [0032] of Patariu, as (similar to a bus) being under control of memory interface 106 to *transfer encrypted/decrypted data buffered in FIFO 110 to memory block 104*. Further, Patariu describes and illustrates a ***complete*** 3DES functional block (112 of Fig. 1 and 208 of Fig. 2), while the "feedback path" required in claim 28 (*a data input node adapted to process the intermediate result data from the data output during a second and third DES processing operation*) between the select switch and *the* ***data input node*** of the ***single DES engine***, would be **internal** to this 3DES block 112, so cannot be the "feedback path" cited in Fig. 1 of Patariu, and thus the deficiency of Patariu can not be made up by Payne.

iii. Neither Patariu nor Payne teach or suggest a single DES engine in combination with a select switch that is coupled to the data output and the data input node of the 3DES engine as recited in claim 28.

Claim 28 further comprises both **a single DES engine** (*e.g.*, 5a of Fig. 1E or 21 of Fig. 1F) **and a select switch coupled to the data output** and **the data input node**, which provides feedback therebetween for the intermediate result data. Instead, Patariu describes and illustrates a complete 3DES functional block (112 of Fig. 1) without this single DES engine feedback. Thus, the structure of Patariu appears to make no provision *to process the intermediate result data from the* ***data output*** *during a second and third DES processing operation* as recited in claim 28 (or the previously presented claim 1).

Accordingly, not all features of independent claim 28 are disclosed by Patariu or Patariu in view of Payne, and favorable acceptance of the claim is respectfully requested.

IV. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP783US.

Respectfully submitted,
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